

A Novel Off-chip Capacitor-less CMOS LDO with Fast Transient Response

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Abstract: - A novel low-dropout (LDO) regulator without external capacitor featuring with fast transient response and low-power dissipation for System-On-Chip (SOC) is proposed in this paper. By introducing an auxiliary feedback path to splits the poles without using a miller compensating scheme, the proposed LDO achieves fast transient response and high stability under all operating conditions. In addition, the transient response is further improved for a buffer stage is utilized. The proposed LDO with a dropout voltage of 200 mV was fabricated in a 0.35um CMOS technology. With the excellent transient response and the highest efficiency about 95%, the proposed LDO has the qualification to be integrated in SOC.

Keywords: - Transient response, Low Dropout regulator(LDO), Auxiliary feedback, Miller compensate

I. INTRODUCTION

Off-chip Capacitor-less LDOs are widely used in cell phone and handheld device^[1]. Owing to stability requirement, the conventional LDO usually needs a large output capacitor which is the main obstacle to fully integrating LDOs in SOC designs. To overcome this issue, capacitor-free LDOs have been studied in [2]-[5]. However, because of the limited on-chip size, the internal on-chip output capacitor is smaller and the ESR is increased. This will lead to severe output voltage changes during a fast-load current transient. Since the output capacitor is small, a dominant pole will no longer be located at the output node, unlike the typical LDO.

Recently, many researchers have proposed various strategies for improving the transient response performance of the off-chip capacitor-less LDO. Using the capacitor coupling effect for the transient response performance^[1-3] and modifying the driver of the power transistor to improve the slew rate have been proposed^[4-8]. However, these topologies are unstable at low currents making their unattractive for real applications. As a result, full range stability and fast-transient LDOs with capacitor-free operation should be developed. Making the correlated tradeoffs on stability, precision, and recovery speed is the main challenge.

In this paper, a novel off-chip capacitor-less LDO with fast transient response and low-power dissipation targeted for SOC is presented. This architecture achieves both fast transient response and high stability under all operating conditions. The organization of this paper is given as follows: Section II presents the topology and structure of the proposed LDO and discusses the overall performance. Circuit implementation and experimental results are given in Sections III and IV, respectively. The conclusion is given in Section V.

II. CIRCUIT AND MECHANISM

Fig.1 shows the proposed LDO topology with a buffer and an auxiliary feedback path constructed by a capacitor C_f and a current amplifier. The high-gain error amplifier (EA) generates the error signal based on a comparison between the reference voltage V_{ref} and the feedback V_{fb} signal from a resistive-divided output voltage. In the output capacitor-less LDO structure, the dominant pole is located in the power transistor M_P gate node, not in the output node. Therefore, a buffer with low input capacitance and a high output resistance characteristic, inserted between the error amplifier and the power transistor, guarantees the stability of the circuit operation. The voltage buffer should improve both the loop-gain bandwidth and slew rate at the gate drive of the power transistor. The auxiliary feedback path, consisting of a capacitor C_f and a current amplifier, connected between the outputs of LDO and EA. Besides, the feedback path of the current control loop is shorter than voltage control loop, so its transient response is much superior to conventional one.

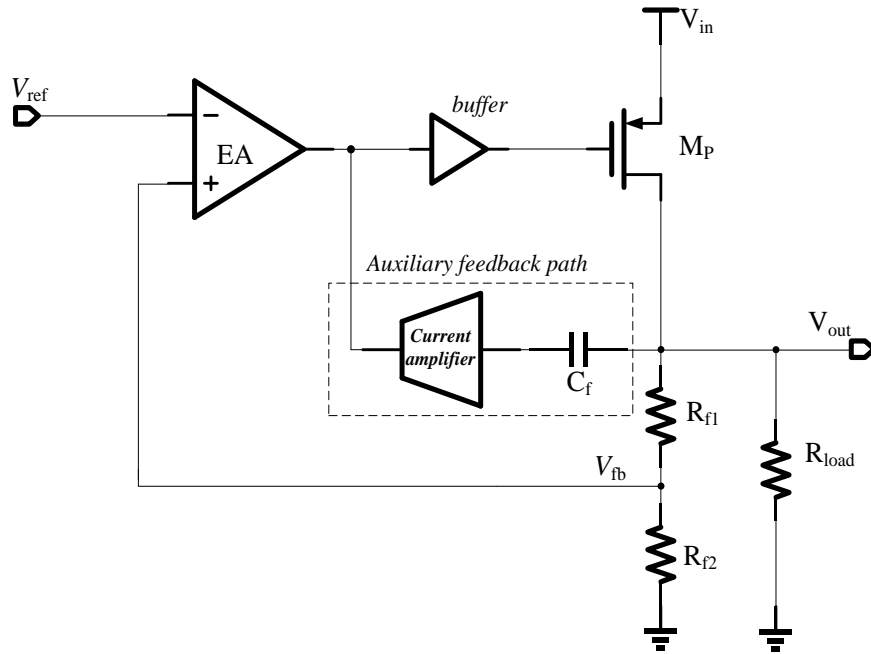


Fig.1 The proposed LDO topology with a buffer and an auxiliary feedback path

Current amplifier, in combination with series compensation capacitor C_f , produce a left-half-plane (LHP) zero, which cancel one of the system non-dominant pole, improving stability. The proposed auxiliary feedback path does not require any additional active components, thereby introducing no additional static power consumption. An additional series resistor in the auxiliary feedback loop allows for accurate placement of the LHP zero. Simple design equations accurately predicting the loop gain, pole-zero locations, and phase margin (PM) are developed. The proposed auxiliary feedback path obviates the feedforward path and introduce LHP zeros, improving the PM, stability, and gain bandwidth.

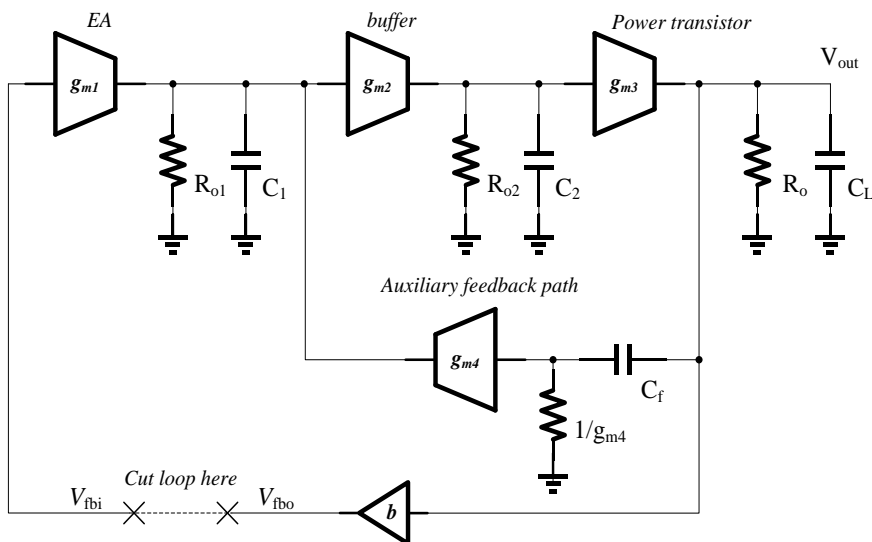


Fig.2 Small-signal diagram of the proposed LDO topology

The open-loop small signal model of the proposed LDO is shown in Fig. 2. It consists mainly of four blocks: a first-stage error amplifier, a second-stage buffer amplifier, an output power transistor, and a dynamic auxiliary feedback path. The dc gain of the LDO regulator is given by the product of the gain of the first-stage amplifier, the second-stage amplifier, the power transistor, and the resistive-divided. The auxiliary feedback compensation capacitor C_f forms the dominant zero of the whole system. The auxiliary feedback block is effectively operating similar to a signal multiplier to magnify the signal passing through C_f to a larger signal.

Assuming that the $C_i \ll C_f$ and C_L , and the poles are widely separated, small-signal analysis yields the transfer function given in equation (1).

$$A_v(s) = \frac{V_{fbo}}{V_{fbi}} \approx \frac{A_{dc}(1+sC_f/g_{m4})}{(1+s/\omega_{p1}) \left[1 + (C_1/g_{m2} + C_f/g_{m3} + C_1/g_{m2}g_{m3}r_o)s + (C_1C_f/g_{m2}g_{m4} + C_1C_f/g_{m2}g_{m3}g_{m4}r_o + C_1C_L/g_{m2}g_{m3})s^2 \right]} \quad (1)$$

Where A_{dc} is the dc voltage gain and can be expressed as

$$A_{dc} = \frac{R_{f2}}{R_{f1} + R_{f2}} g_{m1}r_{o1}g_{m2}r_{o2}g_{m3}r_o \quad (2)$$

The dominant pole ω_p and the dominant LHP zeros are given by:

$$\omega_{p1} = g_{m2}g_{m3}r_{o1}r_{o2}r_o C_f \quad (3)$$

$$\omega_{z1} = -g_{m4}/C_f \quad (4)$$

By introducing an auxiliary feedback path to splits the poles and create a LHP zero, the proposed LDO structure achieves fast transient response and high stability.

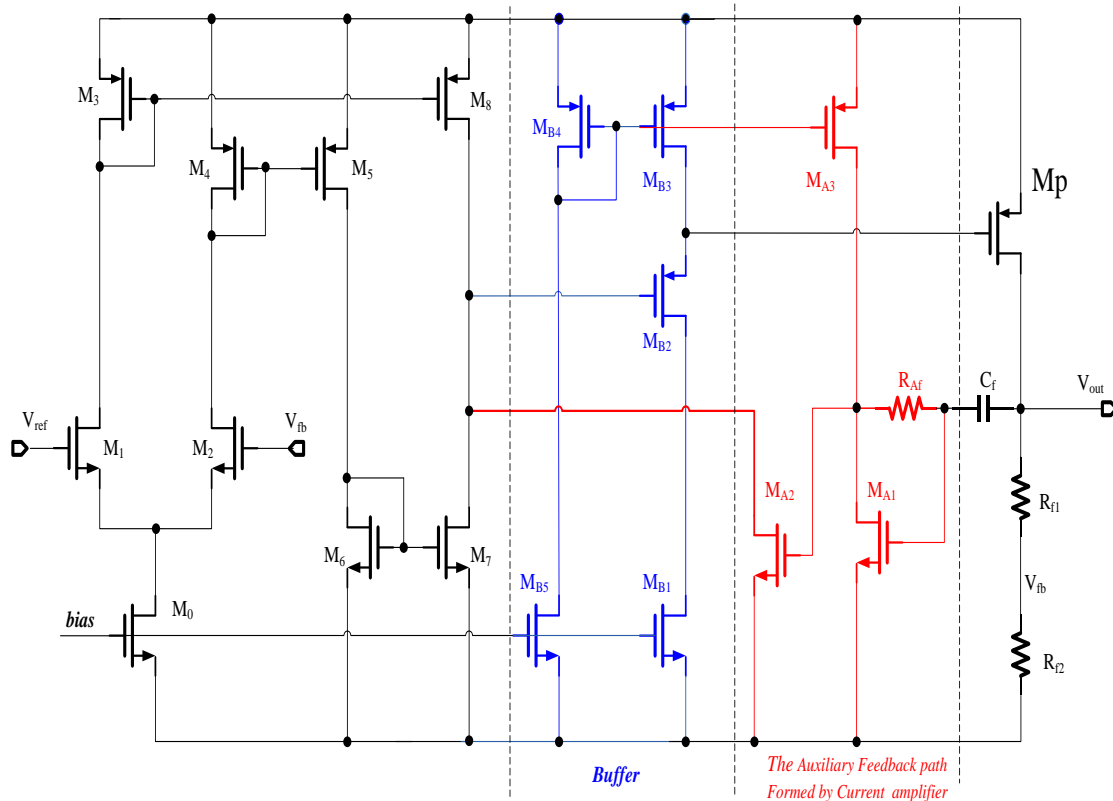


Fig.3 Transistor-level implementation of the proposed LDO

The transistor-level of the proposed off-chip capacitor-less CMOS LDO is shown in Fig.3. The error amplifier (EA) is realized by a typical two stages OTA ($M_0 \sim M_8$) in order to obtain high-gain. The introduced auxiliary feedback circuit is constructed by the current amplifier which is mainly composed by and transistors M_{A1} , M_{A2} and M_{A3} . And the buffer inserted between EA and the power MOS M_p is made up of M_{B1} , M_{B2} and M_{B3} . Where M_{B2} as a source follower with two adaptive loads.

III. RESULTS AND DISCUSSION

The proposed LDO circuit was fabricated with in a 0.35um CMOS technology. Simulation and test results are shown and discussed in this part.

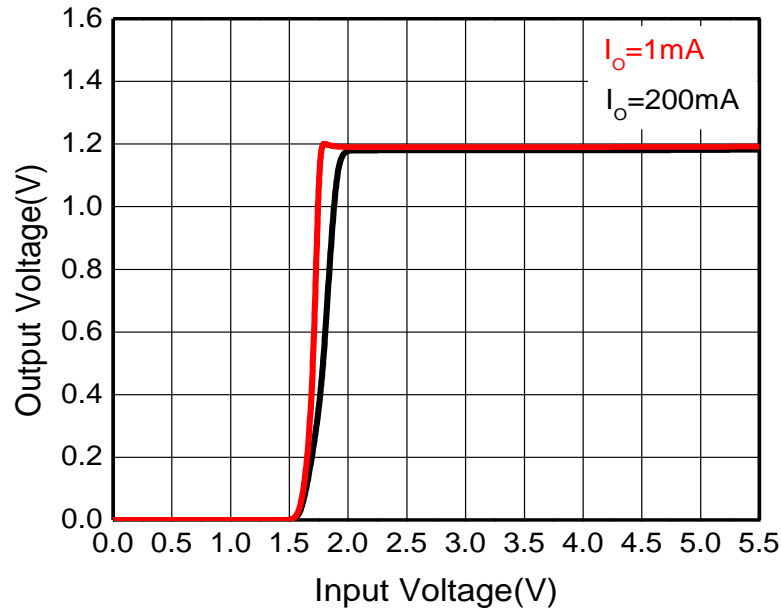


Fig.4 Output Voltage vs Input Voltage

Fig.4 shows the output voltage versus the input voltage. As can be seen, the output voltage is about 1.2V under the condition whenever I_{out} is 1mA or 200mA. The only difference is that the loop response is faster in the light condition which is accordance with the principle. The correctness and feasibility of the proposed feedforward control technique using in the LDO circuit is verified by the test results shown in Fig.5. As shown in Fig.6 (a) $V_{IN}=2.5V-5V$, $I_{OUT}=1mA$ (CH2: V_{OUT} , CH1: V_{IN}), and in (b) $V_{IN}=2.5V$, $V_{OUT}=1.2V$, $I_O=1mA-300mA$ (CH2: V_{OUT} , CH4: I_{OUT}). Experimental results show that the proposed capacitor-less LDO exceeds the current published works in both transient response and ac stability. The architecture is also less sensitive to process variation and loading conditions. Thus, the presented capacitor-less LDO is suitable for SOC solutions.

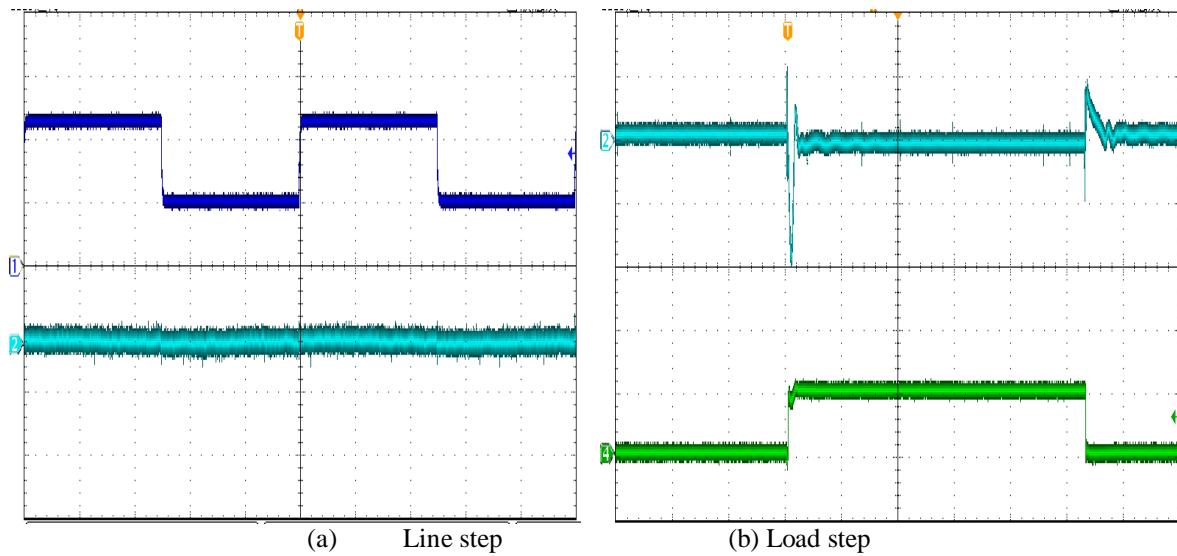


Fig.5 Measurement transient response of the LDO

IV. CONCLUSION

This paper presents a novel current-mode controlled UVLO circuit for DC-DC power management systems. Not only does the proposed UVLO circuit have a compact structure, but also it provides a fast response speed and low temperature coefficient threshold voltages. Simulation results verify the correctness of the theoretical analysis and the feasibility of the proposed circuit.

ACKNOELEDGMENT

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